

## Data Sheet

## ADuM3210/ADuM3211

### FEATURES

Enhanced system-level ESD performance per IEC 61000-4-x

High temperature operation: 125°C

Default low output

Narrow body, RoHS-compliant, 8-lead SOIC

Low power operation

5 V operation

1.7 mA per channel maximum @ 0 Mbps to 2 Mbps

3.7 mA per channel maximum @ 10 Mbps

7.0 mA per channel maximum @ 25 Mbps

3 V operation

1.5 mA per channel maximum @ 0 Mbps to 2 Mbps

2.5 mA per channel maximum @ 10 Mbps

4.7 mA per channel maximum @ 25 Mbps

3 V/5 V level translation

High data rate: dc to 25 Mbps (NRZ)

Precise timing characteristics

3 ns maximum pulse-width distortion at 5 V operation

3 ns maximum channel-to-channel matching

High common-mode transient immunity: >25 kV/μs

Safety and regulatory approvals

UL recognition: 2500 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice #5A

VDE Certificate of Conformity

DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12

$V_{IORM} = 560$  V peak

Qualified for automotive applications

### APPLICATIONS

Size-critical multichannel isolation

SPI interface/data converter isolation

RS-232/RS-422/RS-485 transceiver isolation

Digital field bus isolation

Gate drive interfaces

Hybrid electric vehicles, battery monitor, and motor drive

### GENERAL DESCRIPTION

The ADuM3210/ADuM3211 are dual-channel, digital isolators based on Analog Devices, Inc., *iCoupler*® technology. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *iCoupler* devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *iCoupler* digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *iCoupler* products. Furthermore, *iCoupler* devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM3210/ADuM3211 isolators provide two independent isolation channels in two channel configurations with data rates up to 25 Mbps (see the Ordering Guide). They operate with 3.3 V or 5 V supply voltages on either side, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The ADuM3210/ADuM3211 isolators have a default output low characteristic in comparison to the ADuM3200/ADuM3201 models. The ADuM3210W and ADuM3211W are automotive grade versions qualified for 125°C operation.

In comparison to the ADuM120x isolator, the ADuM3210/ADuM3211 isolators contain various circuit and layout changes providing increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, and surge). The precise capability in these tests for either the ADuM120x or ADuM3210/ADuM3211 products is strongly determined by the design and layout of the user's board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

### FUNCTIONAL BLOCK DIAGRAMS

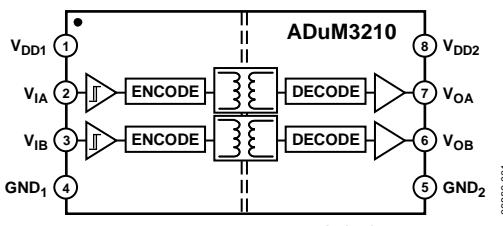


Figure 1. ADuM3210 Functional Block Diagram

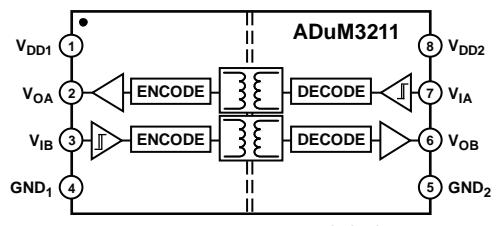


Figure 2. ADuM3211 Functional Block Diagram

Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,239.

Rev. F

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## REVISION HISTORY

### 2/12—Rev. E to Rev. F

Created Hyperlink for Safety and Regulatory Approvals	
Entry in Features Section .....	1
Change to PC Board Layout Section .....	16

### 11/11—Rev. D to Rev. E

Changes to Table 1, Pulse Width Parameter .....	3
Changes to Table 4, Pulse Width Parameter .....	4
Changes to Table 7, Pulse Width Parameter .....	5
Changes to Table 10, Pulse Width Parameter .....	6

### 6/11—Rev. C to Rev. D

Changes to Features Section, Application Section, and General Description Section .....	1
Changes to Propagation Delay Skew Parameter, Table 1; Opposing-Direction Parameter, Table 1; and Quiescent Output Supply Current Parameter, Table 3 .....	3
Changes to Opposing-Direction Parameter, Table 4 .....	4
Changes to Opposing-Direction Parameter, Table 7 and Logic Low Input Threshold Parameter, Table 9 .....	5
Changes to Propagation Delay Skew Parameter, Table 10 and Changes to Table 12 .....	6
Changes to Table 13, Table 14, and Quiescent Output Supply Current Parameter, Table 15 .....	7
Changes to Table 16 and Table 17 .....	8
Changes to Table 19, Table 20, and Logic Low Input Threshold Parameter, Table 21 .....	9

Changes to Table 22, Table 23, and Table 24 .....	10
Changes to Side 1 Current Parameter, Table 28; Side 2 Current Parameter, Table 28; and Table 29 .....	12
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Changes to Figure 9, Figure 10, and Figure 11 Captions .....	15
Changes to Ordering Guide .....	20
Added Automotive Products Section .....	20

### 9/09—Rev. B to Rev. C

Added ADuM3210A and ADuM3211A .....	Throughout
Changes to General Description Section .....	1
Reformatted Electrical Characteristics Tables .....	3
Moved Truth Tables Section .....	14
Changes to Ordering Guide .....	20

### 7/09—Rev. A to Rev. B

Added ADuM3211 .....	Throughout
Changes to Specifications Section .....	3
Added Table 16 .....	19
Added Figure 5 and Table 18 .....	20
Added Figure 11 .....	21
Changes to Power Consumption Section .....	23
Changes to Ordering Guide .....	25

### 9/08—Revision A: Initial Version

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS—5 V, 105°C OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	A Grade			B Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	20		50	20		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			5			3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW								Within PWD limit
ADuM3210		1000			22			ns	
ADuM3211		1000			33			ns	
Propagation Delay Skew	$t_{PSK}$			20			18	ns	Between any two units
Channel Matching									
Codirectional	$t_{PSKCD}$			5			3	ns	
Opposing-Direction	$t_{PSKOD}$			20			18	ns	
Output Rise/Fall Time	$t_R/t_F$		2.5			2.5		ns	10% to 90%

Table 2.

Parameter	Symbol	1 Mbps—A Grade, B Grade			10 Mbps—B Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									
ADuM3210	$I_{DD1}$		1.3	1.7		3.5	4.6	mA	
	$I_{DD2}$		1.0	1.6		1.7	2.8	mA	
ADuM3211	$I_{DD1}$		1.1	1.5		2.6	3.4	mA	
	$I_{DD2}$		1.3	1.8		3.1	4.0	mA	

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	0.7 $V_{DDX}$			V	
Logic Low Input Threshold	$V_{IL}$			0.3 $V_{DDX}$	V	
Logic High Output Voltages	$V_{OH}$	$V_{DDX} - 0.1$	5.0		V	
		$V_{DDX} - 0.5$	4.8		V	
Logic Low Output Voltages	$V_{OL}$		0.0	0.1	V	
			0.2	0.4	V	
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.4	0.8	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		$\text{mA}/\text{Mbps}$	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		$\text{mA}/\text{Mbps}$	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		$\text{kV}/\mu\text{s}$	$V_{lx} = V_{DDX}, V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$		1.2		Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—3 V, 105°C OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.0$  V. Minimum/maximum specifications apply over the entire recommended operation range: ADuM3210 supply voltages  $2.7 \text{ V} \leq V_{DD1} \leq 3.6 \text{ V}$ ,  $2.7 \text{ V} \leq V_{DD2} \leq 3.6 \text{ V}$ ; ADuM3211 supply voltages  $3.0 \text{ V} \leq V_{DD1} \leq 3.6 \text{ V}$ ,  $3.0 \text{ V} \leq V_{DD2} \leq 3.6 \text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15 \text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	A Grade			B Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	$t_{PLH}, t_{PLH}$	20		60	20		60	ns	50% input to 50% output
Pulse Width Distortion	PWD								
ADuM3210				5			3	ns	$ t_{PLH} - t_{PLH} $
ADuM3211				6			4	ns	$ t_{PLH} - t_{PLH} $
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW								Within PWD limit
ADuM3210		1000			22			ns	
ADuM3211		1000			33			ns	
Propagation Delay Skew	$t_{PSK}$			29			22	ns	Between any two units
Channel Matching									
Codirectional	$t_{PSKCD}$			5			3	ns	
Opposing-Direction	$t_{PSKOD}$			29			20	ns	
Output Rise/Fall Time	$t_R/t_F$		3.0			3.0		ns	10% to 90%

Table 5.

Parameter	Symbol	1 Mbps—A Grade, B Grade			10 Mbps—B Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									
ADuM3210	$I_{DD1}$		0.8	1.3		2.0	3.2	mA	
	$I_{DD2}$		0.7	1.0		1.1	1.7	mA	
ADuM3211	$I_{DD1}$		0.7	1.3		1.5	2.1	mA	
	$I_{DD2}$		0.8	1.6		1.9	2.4	mA	

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	0.7 $V_{DDX}$			V	
Logic Low Input Threshold	$V_{IL}$			0.3 $V_{DDX}$	V	
Logic High Output Voltages	$V_{OH}$	$V_{DDX} - 0.1$	3.0		V	$I_{ox} = -20 \mu\text{A}, V_{lx} = V_{lxH}$
		$V_{DDX} - 0.5$	2.8		V	$I_{ox} = -4 \text{ mA}, V_{lx} = V_{lxH}$
Logic Low Output Voltages	$V_{OL}$		0.0	0.1	V	$I_{ox} = 20 \mu\text{A}, V_{lx} = V_{lxL}$
			0.2	0.4	V	$I_{ox} = 4 \text{ mA}, V_{lx} = V_{lxL}$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0 \text{ V} \leq V_{lx} \leq V_{DDX}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		$\text{mA}/\text{Mbps}$	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		$\text{mA}/\text{Mbps}$	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		$\text{kV}/\mu\text{s}$	$V_{lx} = V_{DDX}, V_{CM} = 1000 \text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$		1.1		Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V, 105°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range: ADuM3210 supply voltages  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ ; ADuM3211 supply voltages  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$ , and CMOS signal levels, unless otherwise noted.

**Table 7.**

<b>Parameter</b>	<b>Symbol</b>	<b>A Grade</b>			<b>B Grade</b>			<b>Unit</b>	<b>Test Conditions</b>
		<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>		
<b>SWITCHING SPECIFICATIONS</b>									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	15		55	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD			5			3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW								Within PWD limit
ADuM3210		1000			22			ns	
ADuM3211		1000			33			ns	
Propagation Delay Skew	$t_{PSK}$			29			22	ns	Between any two units
Channel Matching									
Codirectional	$t_{PSKCD}$			5			3	ns	
Opposing-Direction	$t_{PSKOD}$			29			20	ns	
Output Rise/Fall Time	$t_R/t_F$		3.0			3.0		ns	10% to 90%

**Table 8.**

<b>Parameter</b>	<b>Symbol</b>	<b>1 Mbps—A Grade, B Grade</b>			<b>10 Mbps—B Grade</b>			<b>Unit</b>	<b>Test Conditions</b>
		<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>		
<b>SUPPLY CURRENT</b>									
ADuM3210	$I_{DD1}$		1.3	1.7		3.5	4.6	mA	
	$I_{DD2}$		0.7	1.0		1.1	1.7	mA	
ADuM3211	$I_{DD1}$		1.1	1.5		2.6	3.4	mA	
	$I_{DD2}$		0.8	1.6		1.9	2.4	mA	

**Table 9. For All Models**

<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Test Conditions</b>
<b>DC SPECIFICATIONS</b>						
Logic High Input Threshold	$V_{IH}$	0.7 $V_{DDX}$			V	
Logic Low Input Threshold	$V_{IL}$			0.3 $V_{DDX}$	V	
Logic High Output Voltages	$V_{OH}$	$V_{DDX} - 0.1$	$V_{DDX}$		V	$I_{ox} = -20\text{ }\mu\text{A}$ , $V_{lx} = V_{lxH}$
		$V_{DDX} - 0.5$	$V_{DDX} - 0.2$		V	$I_{ox} = -4\text{ mA}$ , $V_{lx} = V_{lxH}$
Logic Low Output Voltages	$V_{OL}$		0.0	0.1	V	$I_{ox} = 20\text{ }\mu\text{A}$ , $V_{lx} = V_{lxL}$
			0.2	0.4	V	$I_{ox} = 4\text{ mA}$ , $V_{lx} = V_{lxL}$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{lx} \leq V_{DDX}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		$\text{mA/Mbps}$	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		$\text{mA/Mbps}$	
<b>AC SPECIFICATIONS</b>						
Common-Mode Transient Immunity <sup>1</sup>	$ \text{CM} $	25	35		$\text{kV}/\mu\text{s}$	$V_{lx} = V_{DDX}$ , $V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$			1.2	Mbps	

<sup>1</sup>  $|\text{CM}|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**ELECTRICAL CHARACTERISTICS—MIXED 3 V/5 V, 105°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 3\text{ V}$ ,  $V_{DD2} = 5.0\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range: ADuM3210 supply voltages  $2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ ; ADuM3211 supply voltages  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

**Table 10.**

<b>Parameter</b>	<b>Symbol</b>	<b>A Grade</b>			<b>B Grade</b>			<b>Unit</b>	<b>Test Conditions</b>
		<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>		
<b>SWITCHING SPECIFICATIONS</b>									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	$t_{PLH}, t_{PLH}$	15		55	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD								
ADuM3210				5			3	ns	$ t_{PLH} - t_{PLH} $
ADuM3211				6			4	ns	$ t_{PLH} - t_{PLH} $
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW								Within PWD limit
ADuM3210		1000			22			ns	
ADuM3211		1000			33			ns	
Propagation Delay Skew	$t_{PSK}$			29			20	ns	Between any two units
Channel Matching									
Codirectional	$t_{PSKCD}$			15			3	ns	
Opposing-Direction	$t_{PSKOD}$			29			22	ns	
Output Rise/Fall Time	$t_R/t_F$		2.5			2.5		ns	10% to 90%

**Table 11.**

<b>Parameter</b>	<b>Symbol</b>	<b>1 Mbps—A Grade, B Grade</b>			<b>10 Mbps—B Grade</b>			<b>Unit</b>	<b>Test Conditions</b>
		<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>		
<b>SUPPLY CURRENT</b>									
ADuM3210	$I_{DD1}$		0.8	1.3		2.0	3.2	mA	
	$I_{DD2}$		1.0	1.6		1.7	2.8	mA	
ADuM3211	$I_{DD1}$		0.7	1.3		1.5	2.1	mA	
	$I_{DD2}$		1.3	1.8		3.1	4.0	mA	

**Table 12. For All Models**

<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Test Conditions</b>
<b>DC SPECIFICATIONS</b>						
Logic High Input Threshold	$V_{IH}$	0.7 $V_{DDX}$			V	
Logic Low Input Threshold	$V_{IL}$			0.3 $V_{DDX}$	V	
Logic High Output Voltages	$V_{OH}$	$V_{DDX} - 0.1$	$V_{DDX}$		V	
		$V_{DDX} - 0.5$	$V_{DDX} - 0.2$		V	
Logic Low Output Voltages	$V_{OL}$		0.0	0.1	V	
			0.2	0.4	V	
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.8	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		$\text{mA}/\text{Mbps}$	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		$\text{mA}/\text{Mbps}$	
<b>AC SPECIFICATIONS</b>						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		$\text{kV}/\mu\text{s}$	$V_{lx} = V_{DDX}, V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$			1.1	Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**ELECTRICAL CHARACTERISTICS—5 V, 125°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

**Table 13.**

<b>Parameter</b>	<b>Symbol</b>	<b>A Grade</b>			<b>B Grade and T Grade</b>			<b>C Grade</b>			<b>Unit</b>	<b>Test Conditions</b>
		<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>		
<b>SWITCHING SPECIFICATIONS</b>												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	20		50	20		50	20		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			5			3			3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6		5				5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	$t_{PSK}$			20			18			18	ns	Between any two units
Channel Matching												
Codirectional	$t_{PSKCD}$			5			3			3	ns	
Opposing-Direction	$t_{PSKOD}$			20			18			18	ns	
Output Rise/Fall Time	$t_R/t_F$		2.5		2.5			2.5			ns	10% to 90%

**Table 14.**

<b>Parameter</b>	<b>Symbol</b>	<b>1 Mbps—A Grade, B Grade, and C Grade</b>			<b>10 Mbps—B Grade, C Grade, and T Grade</b>			<b>25 Mbps—C Grade</b>			<b>Unit</b>	<b>Test Conditions</b>
		<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>		
<b>SUPPLY CURRENT</b>												
ADuM3210	$I_{DD1}$		1.3	1.7		3.5	4.6		6.6	9.0	mA	
	$I_{DD2}$		1.0	1.6		1.7	2.8		3.7	4.5	mA	
ADuM3211	$I_{DD1}$		1.1	1.5		2.6	3.4		5.3	7.5	mA	
	$I_{DD2}$		1.3	1.8		3.1	4.0		5.9	8.0	mA	

**Table 15. For All Models**

<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Test Conditions</b>
<b>DC SPECIFICATIONS</b>						
Logic High Input Threshold	$V_{IH}$		0.7 $V_{DDX}$		V	
Logic Low Input Threshold	$V_{IL}$			0.3 $V_{DDX}$	V	
Logic High Output Voltages	$V_{OH}$	$V_{DDX} - 0.1$	5.0		V	$I_{ox} = -20\text{ }\mu\text{A}, V_{lx} = V_{lxH}$
		$V_{DDX} - 0.5$	4.8		V	$I_{ox} = -4\text{ mA}, V_{lx} = V_{lxH}$
Logic Low Output Voltages	$V_{OL}$		0.0	0.1	V	$I_{ox} = 20\text{ }\mu\text{A}, V_{lx} = V_{lxL}$
			0.2	0.4	V	$I_{ox} = 4\text{ mA}, V_{lx} = V_{lxL}$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{lx} \leq V_{DDX}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.4	0.8	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		$\text{mA}/\text{Mbps}$	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		$\text{mA}/\text{Mbps}$	
<b>AC SPECIFICATIONS</b>						
Common-Mode Transient Immunity <sup>1</sup>	$ \text{CM} $	25	35		$\text{kV}/\mu\text{s}$	$V_{lx} = V_{DDX}, V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$		1.2		Mbps	

<sup>1</sup>  $|\text{CM}|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—3 V, 125°C OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.0\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 16.

Parameter	Symbol	A Grade			B Grade and T Grade			C Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{TPLH}$	20	60		20	60		20	60		ns	50% input to 50% output
Pulse Width Distortion	PWD			6			4			4	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6		5				5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	$t_{PSK}$			29			22			22	ns	Between any two units
Channel Matching												
Codirectional	$t_{PSKCD}$			5			3			3	ns	
Opposing-Direction	$t_{PSKOD}$			29			20			20	ns	
Output Rise/Fall Time	$t_R/t_F$		3.0		3.0				3.0		ns	10% to 90%

Table 17.

Parameter	Symbol	1 Mbps—A Grade, B Grade, and C Grade			10 Mbps—B Grade, C Grade, and T Grade			25 Mbps—C Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
ADuM3210	$I_{DD1}$	0.8	1.3		2.0	3.2		3.9	5.5		mA	
	$I_{DD2}$	0.7	1.0		1.1	1.7		2.4	3.0		mA	
ADuM3211	$I_{DD1}$	0.7	1.3		1.5	2.1		3.1	4.5		mA	
	$I_{DD2}$	0.8	1.6		1.9	2.4		3.5	5.0		mA	

Table 18. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	0.7 $V_{DDX}$			V	
Logic Low Input Threshold	$V_{IL}$			0.3 $V_{DDX}$	V	
Logic High Output Voltages	$V_{OH}$	$V_{DDX} - 0.1$	3.0		V	$I_{ox} = -20\text{ }\mu\text{A}, V_{lx} = V_{lxH}$
		$V_{DDX} - 0.5$	2.8		V	$I_{ox} = -4\text{ mA}, V_{lx} = V_{lxH}$
Logic Low Output Voltages	$V_{OL}$		0.0	0.1	V	$I_{ox} = 20\text{ }\mu\text{A}, V_{lx} = V_{lxL}$
			0.2	0.4	V	$I_{ox} = 4\text{ mA}, V_{lx} = V_{lxL}$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{lx} \leq V_{DDX}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		$\text{mA/Mbps}$	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		$\text{mA/Mbps}$	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		$\text{kV}/\mu\text{s}$	$V_{lx} = V_{DDX}, V_{CM} = 1000\text{ V},$ $\text{transient magnitude} = 800\text{ V}$
Refresh Rate	$f_r$			1.1	Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V, 125°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

**Table 19.**

<b>Parameter</b>	<b>Symbol</b>	<b>A Grade</b>			<b>B Grade and T Grade</b>			<b>C Grade</b>			<b>Unit</b>	<b>Test Conditions</b>
		<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>		
<b>SWITCHING SPECIFICATIONS</b>												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	15		55	15		55	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD			5			3			3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6		5				5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	$t_{PSK}$			29			22			22	ns	Between any two units
Channel Matching												
Codirectional	$t_{PSKCD}$			5			3			3	ns	
Opposing-Direction	$t_{PSKOD}$			29			20			20	ns	
Output Rise/Fall Time	$t_R/t_F$		3.0		3.0			3.0			ns	10% to 90%

**Table 20.**

<b>Parameter</b>	<b>Symbol</b>	<b>1 Mbps—A Grade, B Grade, and C Grade</b>			<b>10 Mbps—B Grade, C Grade, and T Grade</b>			<b>25 Mbps—C Grade</b>			<b>Unit</b>	<b>Test Conditions</b>
		<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>		
<b>SUPPLY CURRENT</b>												
ADuM3210	$I_{DD1}$		1.3	1.7		3.5	4.6		6.6	9.0	mA	
	$I_{DD2}$		0.7	1.0		1.1	1.7		2.4	3.0	mA	
ADuM3211	$I_{DD1}$		1.1	1.5		2.6	3.4		5.3	7.5	mA	
	$I_{DD2}$		0.8	1.6		1.9	2.4		3.5	5.0	mA	

**Table 21. For All Models**

<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Test Conditions</b>
<b>DC SPECIFICATIONS</b>						
Logic High Input Threshold	$V_{IH}$	0.7 $V_{DDX}$			V	
Logic Low Input Threshold	$V_{IL}$			0.3 $V_{DDX}$	V	
Logic High Output Voltages	$V_{OH}$	$V_{DDX} - 0.1$	$V_{DDX}$		V	$I_{ox} = -20\text{ }\mu\text{A}, V_{lx} = V_{lxH}$
		$V_{DDX} - 0.5$	$V_{DDX} - 0.2$		V	$I_{ox} = -4\text{ mA}, V_{lx} = V_{lxH}$
Logic Low Output Voltages	$V_{OL}$	0.0	0.1		V	$I_{ox} = 20\text{ }\mu\text{A}, V_{lx} = V_{lxL}$
		0.2	0.4		V	$I_{ox} = 4\text{ mA}, V_{lx} = V_{lxL}$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{lx} \leq V_{DDX}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$	0.4	0.8		mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$	0.3	0.5		mA	
Dynamic Input Supply Current	$I_{DDI(D)}$	0.19			$\text{mA}/\text{Mbps}$	
Dynamic Output Supply Current	$I_{DDO(D)}$	0.03			$\text{mA}/\text{Mbps}$	
<b>AC SPECIFICATIONS</b>						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		$\text{kV}/\mu\text{s}$	$V_{lx} = V_{DDX}, V_{CM} = 1000\text{ V},$ transient magnitude = 800 V
Refresh Rate	$f_r$		1.2		Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—MIXED 3 V/5 V, 125°C OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 3\text{ V}$ ,  $V_{DD2} = 5.0\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 22.

Parameter	Symbol	A Grade			B Grade and T Grade			C Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{TPLH}$	15		55	15		55	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD			6			4			4	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	$t_{PSK}$			29			22			22	ns	Between any two units
Channel Matching												
Codirectional	$t_{PSKCD}$			15			3			3	ns	
Opposing-Direction	$t_{PSKOD}$			29			20			20	ns	
Output Rise/Fall Time	$t_R/t_F$		2.5			2.5			2.5		ns	10% to 90%

Table 23.

Parameter	Symbol	1 Mbps—A Grade, B Grade, and C Grade			10 Mbps—B Grade, C Grade, and T Grade			25 Mbps—C Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
ADuM3210	$I_{DD1}$		0.8	1.3		2.0	3.2		3.9	5.5	mA	
	$I_{DD2}$		1.0	1.6		1.7	2.8		3.7	4.5	mA	
ADuM3211	$I_{DD1}$		0.7	1.3		1.5	2.1		3.1	4.5	mA	
	$I_{DD2}$		1.3	1.8		3.1	4.0		5.9	8.0	mA	

Table 24. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	0.7 $V_{DDX}$			V	
Logic Low Input Threshold	$V_{IL}$			0.3 $V_{DDX}$	V	
Logic High Output Voltages	$V_{OH}$	$V_{DDX} - 0.1$	$V_{DDX}$		V	$I_{ox} = -20\text{ }\mu\text{A}, V_{lx} = V_{lxH}$
		$V_{DDX} - 0.5$	$V_{DDX} - 0.2$		V	$I_{ox} = -4\text{ mA}, V_{lx} = V_{lxH}$
Logic Low Output Voltages	$V_{OL}$		0.0	0.1	V	$I_{ox} = 20\text{ }\mu\text{A}, V_{lx} = V_{lxL}$
			0.2	0.4	V	$I_{ox} = 4\text{ mA}, V_{lx} = V_{lxL}$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{lx} \leq V_{DDX}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.8	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		$\text{mA/Mbps}$	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		$\text{mA/Mbps}$	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		$\text{kV}/\mu\text{s}$	$V_{lx} = V_{DDX}, V_{CM} = 1000\text{ V},$ $\text{transient magnitude} = 800\text{ V}$
Refresh Rate	$f_r$		1.1		Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## PACKAGE CHARACTERISTICS

Table 25.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	
Capacitance (Input-to-Output) <sup>1</sup>	C <sub>I-O</sub>		1.0		pF	f = 1 MHz
Input Capacitance	C <sub>I</sub>		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ <sub>JCI</sub>		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ <sub>JCO</sub>		41		°C/W	

<sup>1</sup> The device is considered a 2-terminal device; Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

## REGULATORY INFORMATION

The ADuM3210/ADuM3211 are approved by the organizations listed in Table 26.

Table 26.

UL	CSA	VDE
Recognized under UL 1577 Component Recognition Program <sup>1</sup>	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 <sup>2</sup>
Single/basic 2500 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage Functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

<sup>1</sup> In accordance with UL 1577, each ADuM3210/ADuM3211 is proof tested by applying an insulation test voltage  $\geq$  3000 V rms for 1 second (current leakage detection limit = 5  $\mu$ A).

<sup>2</sup> In accordance with DIN V VDE V 0884-10, each ADuM3210/ADuM3211 is proof tested by applying an insulation test voltage  $\geq$  1050 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (\*) marking on the component designates DIN V VDE V 0884-10 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 27.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

**DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS**

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (\*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

**Table 28.**

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage $\leq 150$ V rms			I to IV	
For Rated Mains Voltage $\leq 300$ V rms			I to III	
For Rated Mains Voltage $\leq 400$ V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		$V_{IORM}$	560	V peak
Input-to-Output Test Voltage, Method B1		$V_{PR}$	1050	V peak
Input-to-Output Test Voltage, Method A		$V_{PR}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.875 = V_{PR}$ , $t_m = 1$ sec, partial discharge $< 5$ pC		896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, partial discharge $< 5$ pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ sec	$V_{TR}$	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		$T_S$	150	°C
Side 1 Current		$I_{S1}$	160	mA
Side 2 Current		$I_{S2}$	170	mA
Insulation Resistance at $T_S$	$V_{IO} = 500$ V	$R_S$	$>10^9$	Ω

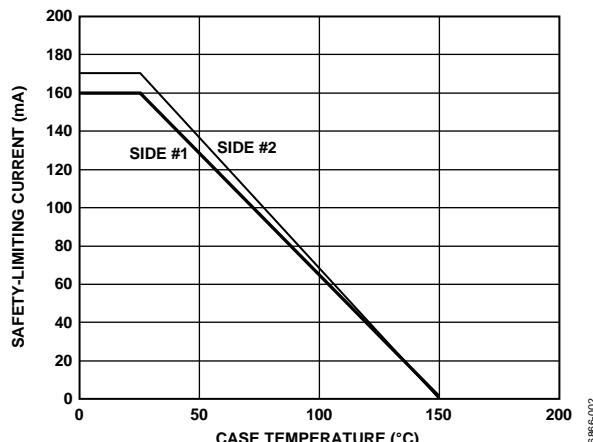


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature per DIN V VDE V 0884-10

**RECOMMENDED OPERATING CONDITIONS****Table 29.**

Parameter	Symbol	Rating
Operating Temperature	$T_A$	-40°C to +105°C
ADuM3210A/ADuM3211A		-40°C to +105°C
ADuM3210B/ADuM3211B		-40°C to +105°C
ADuM3210T/ADuM3211T		-40°C to +125°C
ADuM3210WA/ADuM3211WA		-40°C to +125°C
ADuM3210WB/ADuM3211WB		-40°C to +125°C
ADuM3210WC/ADuM3211WC		-40°C to +125°C
Supply Voltages <sup>1</sup>	$V_{DD1}, V_{DD2}$	
ADuM3210A/ADuM3211A		2.7 V to 5.5 V
ADuM3210B/ADuM3211B		2.7 V to 5.5 V
ADuM3210T/ADuM3211T		3 V to 5.5 V
ADuM3210WA/ADuM3211WA		3 V to 5.5 V
ADuM3210WB/ADuM3211WB		3 V to 5.5 V
ADuM3210WC/ADuM3211WC		3 V to 5.5 V
Maximum Input Signal Rise and Fall Times		1 ms

<sup>1</sup> All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

## ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 30.

Parameter	Symbol	Rating
Storage Temperature	T <sub>ST</sub>	−55°C to +150°C
Ambient Operating Temperature	T <sub>A</sub>	−40°C to +125°C
Supply Voltages <sup>1</sup>	V <sub>DD1</sub> , V <sub>DD2</sub>	−0.5 V to +7.0 V
Input Voltage <sup>1,2</sup>	V <sub>IA</sub> , V <sub>IB</sub>	−0.5 V to V <sub>DD1</sub> + 0.5 V
Output Voltage <sup>1,2</sup>	V <sub>OA</sub> , V <sub>OB</sub>	−0.5 V to V <sub>DD2</sub> + 0.5 V
Average Output Current per Pin <sup>3</sup>	I <sub>O</sub>	−22 mA to +22 mA
Common-Mode Transients <sup>4</sup>	CM <sub>H</sub> , CM <sub>L</sub>	−100 kV/μs to +100 kV/μs

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> V<sub>DD1</sub> and V<sub>DD2</sub> refer to the supply voltages on the input and output sides of a given channel, respectively.

<sup>3</sup> See Figure 3 for information on maximum allowable current for various temperatures.

<sup>4</sup> Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 31. Maximum Continuous Working Voltage<sup>1</sup>

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

<sup>1</sup> Refers to continuous voltage magnitude imposed across the insulation barrier. See the Insulation Lifetime eWf[a] for more details.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

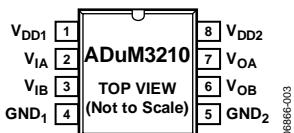


Figure 4. ADuM3210 Pin Configuration



Figure 5. ADuM3211 Pin Configuration

Table 32. ADuM3210 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	V <sub>IA</sub>	Logic Input A.
3	V <sub>IB</sub>	Logic Input B.
4	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
5	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
6	V <sub>OB</sub>	Logic Output B.
7	V <sub>OA</sub>	Logic Output A.
8	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

Table 33. ADuM3211 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	V <sub>OA</sub>	Logic Output A.
3	V <sub>IB</sub>	Logic Input B.
4	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
5	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
6	V <sub>OB</sub>	Logic Output B.
7	V <sub>IA</sub>	Logic Input A.
8	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

## TRUTH TABLES

Table 34. ADuM3210 Truth Table (Positive Logic)

V <sub>IA</sub> Input <sup>1</sup>	V <sub>IB</sub> Input <sup>1</sup>	V <sub>DD1</sub> State	V <sub>DD2</sub> State	V <sub>OA</sub> Output <sup>1</sup>	V <sub>OB</sub> Output <sup>1</sup>	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	L	L	Outputs return to the input state within 1 $\mu$ s of V <sub>DD1</sub> power restoration
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 $\mu$ s of V <sub>DD2</sub> power restoration

<sup>1</sup> H refers to a high logic, and L refers to a low logic.

Table 35. ADuM3211 Truth Table (Positive Logic)

V <sub>IA</sub> Input <sup>1</sup>	V <sub>IB</sub> Input <sup>1</sup>	V <sub>DD1</sub> State	V <sub>DD2</sub> State	V <sub>OA</sub> Output <sup>1</sup>	V <sub>OB</sub> Output <sup>1</sup>	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	L	Outputs return to the input state within 1 $\mu$ s of V <sub>DD1</sub> power restoration
X	X	Powered	Unpowered	L	Indeterminate	Outputs return to the input state within 1 $\mu$ s of V <sub>DD2</sub> power restoration

<sup>1</sup> H refers to a high logic, L refers to a low logic, and X refers to high or low logic, don't care.

## TYPICAL PERFORMANCE CHARACTERISTICS

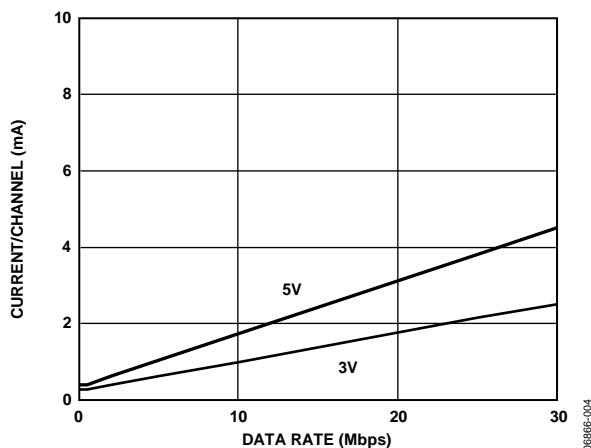


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

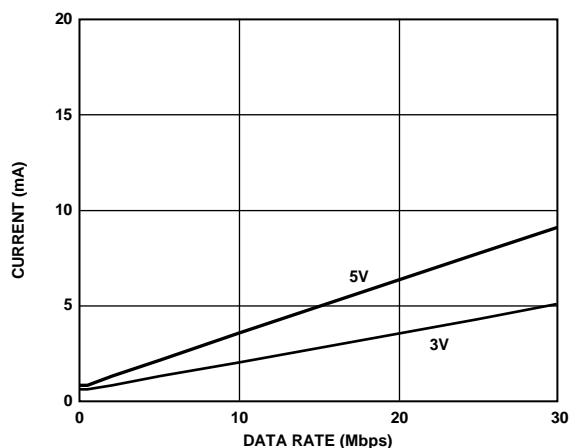


Figure 9. ADuM3210 Typical  $I_{DD1}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

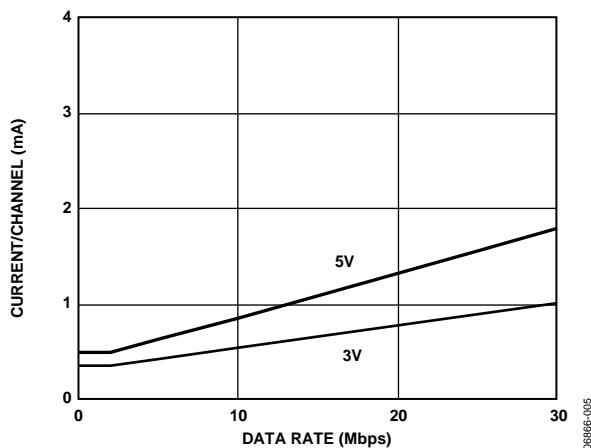


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

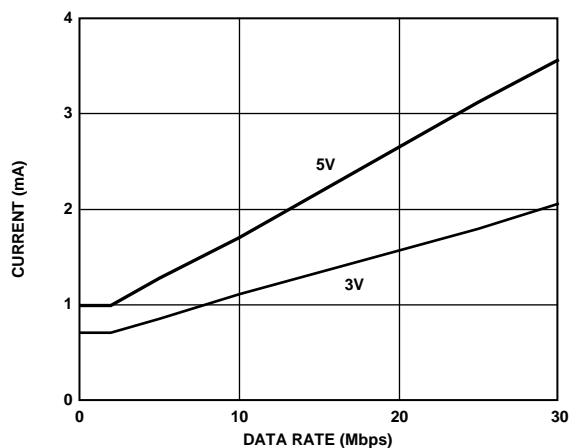


Figure 10. ADuM3210 Typical  $I_{DD2}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

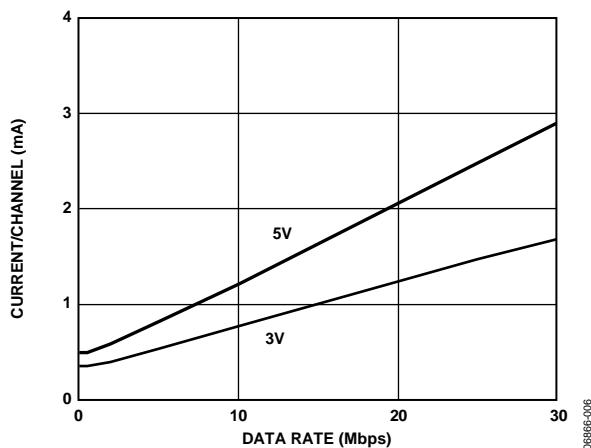


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

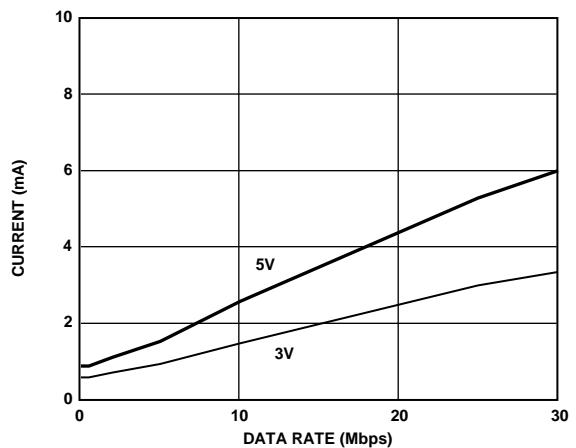


Figure 11. ADuM3211 Typical  $I_{DD1}$  or  $I_{DD2}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

## APPLICATIONS INFORMATION

### PC BOARD LAYOUT

The ADuM3210/ADuM3211 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins. The capacitor value should be between 0.01  $\mu$ F and 0.1  $\mu$ F. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

See the [AN-1109 Application Note](#) for board layout guidelines.

### SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design, which varies widely by application. The ADuM3210/ADuM3211 incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include:

- ESD protection cells were added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices is minimized by use of a guarding and isolation technique between the PMOS and NMOS devices.
- Areas of high electric field concentration are eliminated using 45° corners on metal traces.
- Supply pin overvoltage is prevented with larger ESD clamps between each supply pin and its respective ground.

While the ADuM3210/ADuM3211 improve system-level ESD reliability, they are no substitute for a robust system-level design. For detailed recommendations on board layout and system-level design, see the [AN-793 Application Note](#), *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

### PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output.

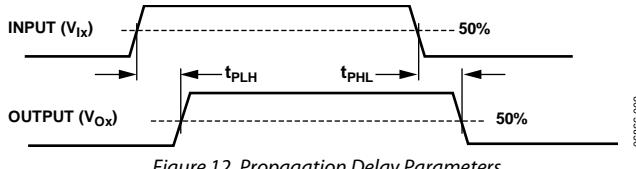


Figure 12. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM3210/ADuM3211 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM3210/ADuM3211 components operating under the same conditions.

### DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 2  $\mu$ s at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5  $\mu$ s, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default state (see Table 34 and Table 35) by the watchdog timer circuit.

The ADuM3210/ADuM3211 are immune to external magnetic fields. The limitation on the ADuM3210/ADuM3211 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM3210/ADuM3211 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2, \quad n = 1, 2, \dots, N$$

where:

$\beta$  is the magnetic flux density (gauss).

$N$  is the number of turns in the receiving coil.

$r_n$  is the radius of the  $n$ th turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM3210/ADuM3211 and an imposed requirement that the induced voltage is at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 13.

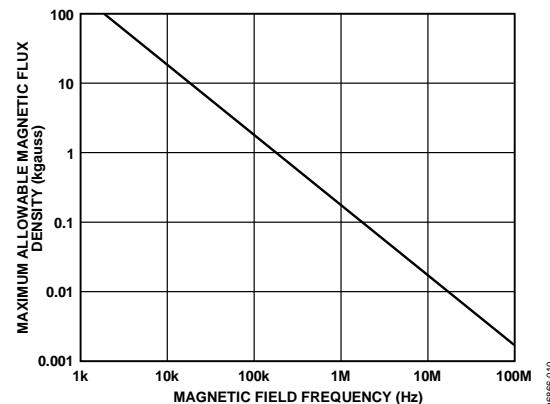


Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and had the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM3210/ADuM3211 transformers. Figure 14 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM3210/ADuM3211 are immune and can be affected only by extremely large currents operated at a high frequency and very close to the component. For the 1 MHz example, a 0.5 kA current would have to be placed 5 mm away from the ADuM3210/ADuM3211 to affect the operation of the component.

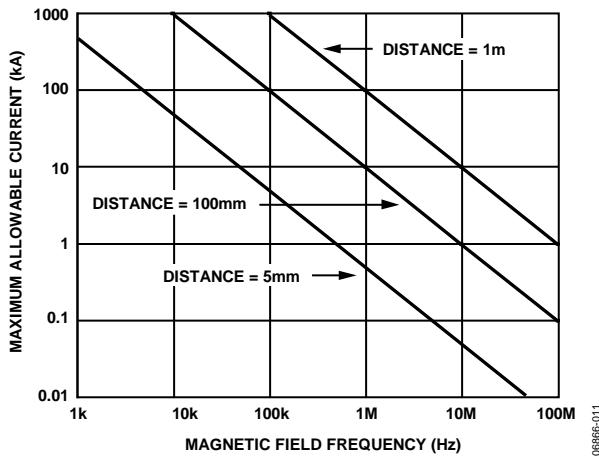


Figure 14. Maximum Allowable Current for Various Current-to-ADuM3210/ADuM3211 Spacings

Note that at combinations of strong magnetic fields and high frequencies, any loops formed by the printed circuit board (PCB) traces may induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

## POWER CONSUMPTION

The supply current at a given channel of the ADuM3210/ADuM3211 isolator is a function of the supply voltage, channel data rate, and channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5f_r$$

where:

$I_{DDI(D)}$ ,  $I_{DDO(D)}$  are the input and output dynamic supply currents per channel (mA/Mbps).

$I_{DDI(Q)}$ ,  $I_{DDO(Q)}$  are the specified input and output quiescent supply currents (mA).

$C_L$  is the output load capacitance (pF).

$V_{DDO}$  is the output supply voltage (V).

$f$  is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

$f_r$  is the input stage refresh rate (Mbps).

To calculate the total  $I_{DD1}$  and  $I_{DD2}$  supply current, the supply currents for each input and output channel corresponding to  $I_{DD1}$  and  $I_{DD2}$  are calculated and totaled.

Figure 6 provides the input supply currents per channel as a function of data rate. Figure 7 and Figure 8 provide the output supply currents per channel as a function of data rate for an unloaded output condition and for a 15 pF output condition, respectively. Figure 9 through Figure 11 provide total  $I_{DD1}$  and  $I_{DD2}$  supply current as a function of data rate for the ADuM3210 and ADuM3211 channel configurations.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the [ADuM3210/ADuM3211](#).

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage.

Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 31 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the [ADuM3210/ADuM3211](#) depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the most stringent. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 31 can be applied while maintaining the 50-year minimum lifetime provided that the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 16 or Figure 17 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 31.

Note that the voltage presented in Figure 16 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

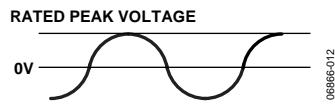


Figure 15. Bipolar AC Waveform

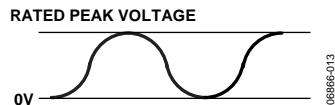


Figure 16. Unipolar AC Waveform

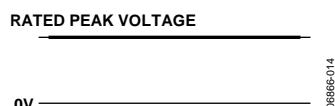
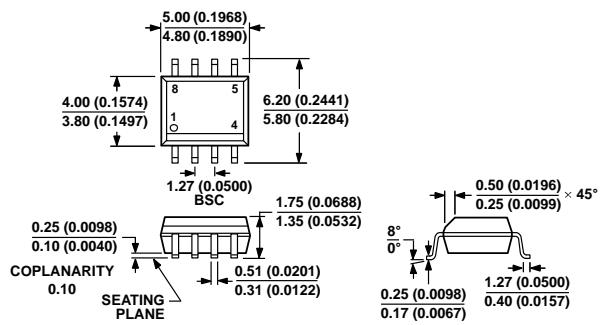


Figure 17. DC Waveform

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407.4

Figure 18. 8-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body (R-8)  
Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model <sup>1, 2</sup>	Number of Inputs, V <sub>DD1</sub> Side	Number of Inputs, V <sub>DD2</sub> Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Option <sup>3</sup>
ADuM3210ARZ	2	0	1	50	5	−40°C to +105°C	R-8
ADuM3210ARZ-RL7	2	0	1	50	5	−40°C to +105°C	R-8
ADuM3210BRZ	2	0	10	50	3	−40°C to +105°C	R-8
ADuM3210BRZ-RL7	2	0	10	50	3	−40°C to +105°C	R-8
ADuM3210TRZ	2	0	10	50	3	−40°C to +125°C	R-8
ADuM3210TRZ-RL7	2	0	10	50	3	−40°C to +125°C	R-8
ADuM3210WARZ	2	0	1	50	5	−40°C to +125°C	R-8
ADuM3210WARZ-RL7	2	0	1	50	5	−40°C to +125°C	R-8
ADuM3210WBRZ	2	0	10	50	3	−40°C to +125°C	R-8
ADuM3210WBRZ-RL7	2	0	10	50	3	−40°C to +125°C	R-8
ADuM3210WCRZ	2	0	25	50	3	−40°C to +125°C	R-8
ADuM3210WCRZ-RL7	2	0	25	50	3	−40°C to +125°C	R-8
ADuM3211ARZ	1	1	1	50	6	−40°C to +105°C	R-8
ADuM3211ARZ-RL7	1	1	1	50	6	−40°C to +105°C	R-8
ADuM3211BRZ	1	1	10	50	4	−40°C to +105°C	R-8
ADuM3211BRZ-RL7	1	1	10	50	4	−40°C to +105°C	R-8
ADuM3211TRZ	1	1	10	50	4	−40°C to +125°C	R-8
ADuM3211TRZ-RL7	1	1	10	50	4	−40°C to +125°C	R-8
ADuM3211WARZ	1	1	1	50	6	−40°C to +125°C	R-8
ADuM3211WARZ-RL7	1	1	1	50	6	−40°C to +125°C	R-8
ADuM3211WBRZ	1	1	10	50	4	−40°C to +125°C	R-8
ADuM3211WBRZ-RL7	1	1	10	50	4	−40°C to +125°C	R-8
ADuM3211WCRZ	1	1	25	50	4	−40°C to +125°C	R-8
ADuM3211WCRZ-RL7	1	1	25	50	4	−40°C to +125°C	R-8

<sup>1</sup> Z = RoHS Compliant Part.<sup>2</sup> W = Qualified for Automotive Applications.<sup>3</sup> R-8 = 8-lead, narrow body SOIC\_N.

## AUTOMOTIVE PRODUCTS

The ADuM3210W/ADuM3211W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.